REMARKS

Claims 1-10 and 19-30 are pending in the application, of which claims 1, 19, 20, 21 and 30 have been amended. No new claims have been added.

Claims 1-10 and 19-30 stand rejected under 35 USC §103(a) as unpatentable over **Tottori** taken with **Buynoski** and **Ono** (all previously applied).

As noted in Applicant's response of November 13, 2003, **Tottori** discloses a semiconductor device with a multi-level interconnection structure having a first conductive layer disposed below a fuse, and formed in the same layer as the first metal wire as a component of multi-level interconnects, and a second conductive layer disposed below the fuse and formed in the same layer as the second metal wire as a component of the multi-level interconnects.

The Examiner has identified partitioned intermediate metal layers 21, 32, 21, 22, 33, 22, 23, 31, 23.

Buynoski discloses a low dielectric semiconductor device with a rigid lined interconnection system.

The Examiner has identified intermediate metals 2 and 3 having partitioned layers.

The first conductive layer in **Tottori** is not connected to a VIA and is provided for absorbing light not absorbed with laser beam irradiated on a fuse 31.

On the other hand, in the present invention, an intermediate metal layer wiring area not to be connected to a VIA is provided for wiring a signal line, a power source, and the like, which is not disclosed in either of the cited references.

The Examiner does not appear to understand the distinction between metal layers and a metal layer wiring area. The metal layers, in both the present invention and the cited references, may be used as wiring to carry electrical signals. However, the present invention is directed to a metal layer wiring area sandwiched between partitioned intermediate metal layers, where the metal layers are connected to the stack VIA and the metal layer wiring area is not connected to the stack VIA. The metal layer wiring area of the present invention does not contain metal; it is a potential through which ordinary wiring may pass through. None of the references teaches, mentions or suggests these areas through which ordinary wiring may pass through.

Accordingly, claims 19, 20, 21 and 30 have been amended to clarify that the intermediate metal layer wiring area is for ordinary wiring.

Furthermore, none of the cited references teaches, mentions or suggests that a connection area is an intersection portion ("CUT23") where the connecting metal layer and the layer to be connected intersect with each other, as disclosed on page 11, lines 22-23 of the specification.

Accordingly, claims 1, 19, 20, 21 and 30 have been amended to recite this distinction..

These issues were discussed, without resolution, in an interview with the Examiner conducted on December 7, 2004.

Thus, the 35 U.S.C. §103(a) rejection should be withdrawn.

Thus, the 35 U.S.C. §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-10 and 19-30, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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